

## ECE 450 Lab Expectations

All labs are required to be completed and turned in. Lab reports must be submitted and demos must be performed at beginning of the next Lab when you submit your prelab e.g. you will demo Lab 2, submit your lab 2 report, and have your Lab 3 prelab checked at the start of Lab 3. **Late labs without a university sanctioned justification will receive a 0 at the TA's discretion. Regardless, all labs must be completed with the demo performed, and report turned in to pass the class.**

### **Prelab (20 pts)**

The prelab must be completed on the first day of the lab. The prelabs form foundation for the lab and it will be difficult to assist any student who has not completed it beforehand. Please ask questions beforehand if you are having difficulty. Some of the prelabs require substantial work; do not put them off until the last minute.

#### *Breakdown*

Completion: 10 pts

Correctness: 10 pts

*A late prelab grade will be reduced by 50%, subject to TA discretion.*

### **Demo - 10 pts (Verilog labs only)**

For Verilog/Quartus labs, you will demonstrate a simulation in Quartus. You will then load the demo onto the FPGA to demonstrate a working hardware solution. The demo must prove the logical correctness of your design. Ensure that the test patterns you choose are adequate, in particular ensure that you demonstrate correctness on corner cases ([https://en.wikipedia.org/wiki/Corner\\_case](https://en.wikipedia.org/wiki/Corner_case)). If the TA is not satisfied you may be asked to come back later to try again.

#### *Breakdown*

Correctness: 5 pts

Explanation: 5 pts

## Report - 70 pts (Verilog Labs) / 80 pts (Cadence Labs)

A well written report should be:

- Clean            The report should be well organized with correct grammar and spelling.
- Clear            Explanations and concepts should be understandable and easy to follow.
- Concise          Points are not awarded for verbosity, please do not turn in a novel.

Using LaTeX is recommended, it is a useful tool and one which is commonly used for writing academic papers and journals. You can use a free online editor, such as Overleaf: <https://www.overleaf.com/>. You do not have to use this but it is a good skill to learn.

### Format

Submit your report in the IEEE Transactions format. You can obtain a Word or LaTeX template for IEEE Transactions journals for your chosen platform by following the URL below. Should you choose to use LaTeX, use the *bare\_jrn.tex* starter file.

<http://ieeauthorcenter.ieee.org/create-your-ieee-article/use-authoring-tools-and-ieee-article-templates/ieee-article-templates/templates-for-transactions/>

The report must contain:

- A. A list of items completed
- B. A list of items not completed (if any)
- C. Lab procedures
- D. Schematics and Verilog models
- E. Simulation results
- F. Analyses and explanations
- G. Conclusions
- H. Answers to questions contained in the lab

### Breakdown

Grammar/Mechanics	5 pts
Introduction (A,B,C)	10 pts
Body (D,E,F)	25 (Verilog) / 35 (Cadence) pts
Conclusion (G)	15 pts
Answers to Questions(H)	15 pts

### Academic Integrity

Academic Integrity is a serious matter. Students may assist each-other in understanding material, but labs must be completed on an individual level. It is one thing to show a classmate a tool or concept, but wholly another to provide them with a solution. Troubleshooting and debugging are skills that students should be learning; *do not fix another student's errors*. Giving hints is OK so long as they are not obvious, e.g. "I think you need to look more closely at this section", or "Are you sure you've used the right tests?" are acceptable. "You need to check for an input of 0" is not. If you're not sure that you can help without cheating, ask the TA. The report is representative of your work and must be written by you, plagiarism will not be tolerated.